WHAT IS CLAIMED IS:

1. A digital AGC circuit used for an address information demodulation circuit for demodulating address information recorded on a DVD by phase modulation of a wobble signal, the digital AGC circuit comprising:

a peak detection circuit for receiving a digitized wobble signal and detecting a peak value in a time period equal to or more than a half period of the wobble signal;

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value; and

a multiplier for multiplying the digitized wobble signal by the gain adjustment coefficient.

2. The digital AGC circuit of Claim 1, further comprising a delay circuit for delaying the wobble signal and supplying the delayed signal to the multiplier.

3. The digital AGC circuit of Claim 1, further comprising a limiter for limiting the gain adjustment coefficient to be supplied from the gain computation circuit to the multiplier to within a fixed range.

4. The digital AGC circuit of Claim 1, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal; and

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter and supplying the detected maximum value to the gain computation circuit.

5. The digital AGC circuit of Claim 1, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal;

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter; and

an absolute value circuit for computing the absolute value of the detected negative peak value and supplying the computed absolute value to the gain computation circuit.

6. The digital AGC circuit of Claim 1, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal;

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter;

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to the output of the one-period counter; and

a selector for selecting either the detected positive peak value or negative peak value and supplying the selected peak value to the gain computation circuit.

7. The digital AGC circuit of Claim 1, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal; and

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter;

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to the output of the one-period counter; and

a difference circuit for computing the difference between the detected positive peak value and negative peak value and supplying the computed difference to the gain computation circuit.

8. The digital AGC circuit of Claim 1, wherein the peak detection circuit comprises:

a half-period counter for counting a half period of the wobble signal; and

a maximum detection circuit for detecting the maximum value in a half period of the wobble signal as a positive peak value according to an output of the half-period counter;

a minimum detection circuit for detecting the minimum value in a half period of the wobble signal as a negative peak value according to the output of the half-period counter;

an adder for adding the detected positive peak value and negative peak value; and

a selector for selecting either the detected positive peak value or negative peak value according to an output of the adder and supplying the selected peak value to the gain computation circuit.

9. The digital AGC circuit of Claim 1, wherein the gain computation circuit includes a divider for dividing a reference value by the peak value detected by the peak detection circuit.

10. The digital AGC circuit of Claim 9, wherein the divider is constructed of a bit shift circuit for performing bit shift division.

11. A digital AGC circuit used for an address information demodulation circuit for demodulating address information recorded on a DVD by phase modulation of a wobble signal, the digital AGC circuit comprising:

a peak detection circuit for receiving an output of the digital AGC circuit and detecting a peak value in a time period equal to or more than a half period of the input;

a gain computation circuit for computing a gain adjustment coefficient from the detected peak value; and

a multiplier for receiving a digitized wobble signal and multiplying the wobble signal by the gain adjustment coefficient.

12. The digital AGC circuit of Claim 11, further comprising an integrator for integrating the gain adjustment coefficient received from the gain computation circuit and supplying the result to the multiplier.

13. The digital AGC circuit of Claim 11, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal; and

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter and supplying the detected maximum value to the gain computation circuit.

14. The digital AGC circuit of Claim 11, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal;

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter; and

an absolute value circuit for computing an absolute value of the detected negative peak value and supplying the computed absolute value to the gain computation circuit.

15. The digital AGC circuit of Claim 11, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal; and

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter;

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter; and

a selector for selecting either the detected positive peak value or negative peak value and supplying the selected peak value to the gain computation circuit.

16. The digital AGC circuit of Claim 11, wherein the peak detection circuit comprises:

a one-period counter for counting one period of the wobble signal; and

a maximum detection circuit for detecting the maximum value in one period of the wobble signal as a positive peak value according to an output of the one-period counter;

a minimum detection circuit for detecting the minimum value in one period of the wobble signal as a negative peak value according to an output of the one-period counter; and

a difference circuit for computing the difference between the detected positive peak value and negative peak value and supplying the computed difference to the gain computation circuit.

17. The digital AGC circuit of Claim 11, wherein the peak detection circuit comprises:

a half-period counter for counting a half period of the wobble signal; and

a maximum detection circuit for detecting the maximum value in a half period of the wobble signal as a positive peak value according to an output of the half-period counter;

a minimum detection circuit for detecting the minimum value in a half period of the wobble signal as a negative peak value according to an output of the half-period counter;

an adder for adding the detected positive peak value and negative peak value; and

a selector for selecting either the detected positive peak value or negative peak value according to an output of the adder and supplying the selected peak value to the gain computation circuit.

18. The digital AGC circuit of Claim 11, wherein the gain computation circuit includes a divider for dividing a reference value by the peak value detected by the peak detection circuit.

19. The digital AGC circuit of Claim 18, wherein the divider is constructed of a bit shift circuit for performing bit shift division.